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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/346,436	07/01/99	HOUSTON T	TI-21004

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EXAMINER	
KIELIN,E	
ART UNIT	**PAPER NUMBER**
2813	4

DATE MAILED: 08/08/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/346,436	Houston
Examiner	**Group Art Unit**
Erik Kielin	2813

☒ Responsive to communication(s) filed on *Jun 21, 2000*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-4, 7-11, and 18-24* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-4, 7-11, and 18-24* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *May 24, 1999* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of claims 1-4, 7-11, and 18-24 in Paper No. 3 is acknowledged

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "bonding region" (as in claim 4) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objections

3. Claims 2 and 8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. A claim cannot depend from itself.

4. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4, which depends from claim 2, recites "said interconnect

structure contacting said bond region through said portion of said electrically insulating layer.." But in claim 2, "said portion of said electrically insulating layer" was broken down and therefore not longer exists; therefore, no connection can exist therethrough.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 7-9 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Electrical interconnect within the "electrically insulating layer" is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Broadly recited claim 7 does not include the critical feature of the invention of providing electrical interconnect within the electrically insulating layer.

7. Claims 18-24 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As presently written, it is not possible to perform the steps recited in claim 18, for the following reason:

In step (c) Examiner is perplexed as to how a "*buried* dielectric" (emphasis added) could be bonded to anything as the term "buried" suggests that the dielectric is completely surrounded by whatever material in which it is buried.

It is also unclear what Applicant means by "spaced from" in step (b). Are the device layer and the substrate already connected through a dielectric which is creating the "space" therebetween? Or are they spaced from each other while awaiting bonding in step (c)? No order of steps is provided.

Claims 18-24 will be examined as best understood by Examiner. Because step (d) seems to indicate that an interface exists in between the interconnect and either of the device and the substrate which is eventually broken down (claim 22), Examiner assumes that what is buried is the interconnect -- not the dielectric. In other words the interconnect is buried by the dielectric as indicated on page 7, lines 7-12.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims **1**-4 and **10**-11, and **18**-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said outer surface" in line 7. There is insufficient antecedent basis for this limitation in the claim. "Surface" should be replaced with --face-- or vice versa.

Claim 10 recites the limitation "the conducting via" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "the electrically conducting via" in 1. There is insufficient antecedent basis for this limitation in the claim.

The term "buried" in claim 18 is a relative term which renders the claim indefinite. The term "buried" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claims 2-4 and 19-24 are rejected for depending from the independent claims 1 and 18, respectively.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims **1**, 3 and **18**-21, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by **Hayashi** (US 5,087,585).

Regarding claims 1-3, Hayashi discloses a method of fabricating an SOI structure which comprises: providing a substrate 21 (Fig. 2B) and a device wafer 16 (Fig. 1D); forming an electrically insulating layer 17 having an electrical interconnect structure 18 therewithin (Fig. 1E); and bonding said electrically insulating layer to the substrate at the bond region 13, a refractory metal bump, wherein the interconnect structure 18 contacts the bond region (Figs. 2B-2C).

Regarding claims 18-21, and 23-24, Hayashi discloses a method of fabricating an integrated circuit comprising: providing a device layer 23 spaced apart from a substrate 21 (Fig. 2E); bonding a buried dielectric 17 with an interconnect 18 to the device layer 23 to form an interface (shown but not labeled in Fig. 2F) therebetween.

See also columns 3-4 and column 5, lines 11-16.

12. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by **Kobayashi** (US 5,573,972).

Kobayashi discloses that it is known in the art to form an SOI structure comprising:

forming a substantially planar surface comprising areas 312 of one of said device layer and said substrate and areas 315a of said electrically insulation layer; and bonding said surface to the other of said substrate wafer and device layer 301. (See Figures 1A-1C; columns 1-2).

13. Claims 10-11 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Wolf** (Silicon Processing for the VLSI Era, Vol. 2).

Examiner notes (1) that no order to the steps has been required and (2) that Applicant has not made clear that the etching of metal removes the metal from within the via that is not on the edge.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims **1**-4 and **18**-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi** in view of **Applicant's admitted prior art**.

Hayashi is applied as above. Hayashi does not disclose applying a voltage across the electrically insulating layer to break down said portion of said electrically insulating layer.

On page 7, lines 7-12, Applicant indicates that it is known in the art to break down oxide by applying voltage across an electrically insulating layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made because native oxide (i.e. the electrically insulating layer) inherently forms on all metals (perhaps with the exception of gold) --particularly Hayashi's refractory metal bump and indium metal pool-- and for the reasons indicate by Applicant.

16. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kobayashi** in view of **Applicant's admitted prior art**.

Kobayashi is applied as above, but does not disclose the limitations of claims 8 and 9. In the last paragraph of page 2 of the specification, Applicant discloses that all of the limitations of claims 8-9 as being known in the art.

Examiner notes that (1) independent claim 7 lacks the major point of the invention which is to provide electrical interconnect within the electrically insulating layer **before** bonding to either of the substrate or device wafer; and (2) dependent claims 8 and 9, which recite the interconnect element, do not require an order for its formation relative to the bonding step, and thereby read on Applicant's admitted prior art, which points out that it is known in the art to form interconnect **after** bonding. Note that the interconnect formed after bonding would still be *in* the insulating layer and contact both the substrate and the device wafer through said insulating layer.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rioult (US 3,787,822) teaches applying a voltage across a dielectric interface 16 between conductive metal layers 12, 15 interface to remove native metal oxide from interconnect material (Abstract).

Any inquiry concerning this communication from examiner should be directed to Erik Kielin whose telephone number is (703) 306-5980. The examiner can normally be reached by telephone on Monday through Thursday 9:00 AM until 7:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for the group is (703) 308-7722 or -7724.

EK

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800

August 3, 2000